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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,527	02/26/2004	Kuo-Chi Tu	67,200-1247	7735

7590 06/10/2005  
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EXAMINER

PRENTY, MARK V

ART UNIT	PAPER NUMBER
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2822

DATE MAILED: 06/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/789,527

Applicant(s)

TU, KUO-CHI

Examiner

MARK V. PRENTY

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 7-20 is/are rejected.
- 7) ☒ Claim(s) 5 and 6 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date February 26, 2004.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

This Office Action is in response to the papers filed on February 26, 2004.

Claims 8-13 and 15-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claims 8-11 are indefinite in reciting, "The method of claim 1," because claim 1 recites a product. Claims 8-11 apparently should depend on independent method claim 7. Claim 12 is indefinite in reciting, "The method of claim 4," because claim 4 recites a product. Claim 12 apparently should depend on claim 11. Claim 13 is indefinite in reciting, "The method of claim 5," because claim 5 recites a product. Claim 13 apparently should depend on claim 12. Claims 15-18 are indefinite in reciting, "The method of claim 1," because claim 1 recites a product. Claims 15-18 apparently should depend on independent method claim 14. Claim 19 is indefinite in reciting, "The method of claim 4," because claim 4 recites a product. Claim 19 apparently should depend on claim 18. Claim 20 is indefinite in reciting, "The method of claim 5," because claim 5 recites a product. Claim 20 apparently should depend on claim 19.

Claims 1, 2, 4, 7-9 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent 6,864,151 to Yan et al. (Yan).

With respect to independent claim 1, Yan discloses an embedded semiconductor product (see the entire patent, including the Figs. 6-9 disclosure, for example) comprising: a semiconductor substrate 302; a first isolation trench 330 adjoining a logic cell active region 312 of the semiconductor substrate; and a second isolation trench 314

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adjoining a memory cell active region 308 of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yan.

With respect to dependent claim 2, Yan's first isolation trench 330 is formed to a depth of from about 2500 to about 5000 angstroms (see column 7, lines 28-31).

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yan.

With respect to dependent claim 4, Yan's product further comprises a first isolation region 324 formed within the first isolation trench 330 and a second isolation region 324a formed within the second isolation trench 314.

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yan.

With respect to independent claim 7, Yan discloses a method for fabricating an embedded semiconductor product (see the entire patent, including the Figs. 6-9 disclosure, for example) comprising: providing a semiconductor substrate 302; forming a first isolation trench 330 adjoining a logic cell active region 312 of the semiconductor substrate; and forming a second isolation trench 314 adjoining a memory cell active region 308 of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench.

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yan.

With respect to dependent claim 8 (which is presumed to depend on independent method claim 7, as per the above rejection of claim 8 under 35 U.S.C. 112, second paragraph), Yan's semiconductor substrate 302 is a silicon semiconductor substrate (see column 6, lines 3-4).

Claim 8 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yan.

With respect to dependent claim 9 (which is presumed to depend on independent method claim 7, as per the above rejection of claim 9 under 35 U.S.C. 112, second paragraph), Yan's first isolation trench 330 is formed to a depth of from about 2500 to about 5000 angstroms (see column 7, lines 28-31).

Claim 9 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yan.

With respect to dependent claim 11 (which is presumed to depend on independent method claim 7, as per the above rejection of claim 11 under 35 U.S.C. 112, second paragraph), Yan's product further comprises a first isolation region 324 formed within the first isolation trench 330 and a second isolation region 324a formed within the second isolation trench 314.

Claim 11 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Yan.

Claims 1-4, 7-11 and 14-18 are rejected under 35 U.S.C. 102(e) as being anticipated by United States Patent 6,833,602 to Mehta.

With respect to independent claim 1, Mehta discloses an embedded semiconductor product (see the entire patent, particularly the Figs. 5-9 disclosure together with the Technical Field, Background and Summary) comprising: a semiconductor substrate 40; a first isolation trench 62 adjoining a logic cell active region of the semiconductor substrate (note column 5, lines 4-7); and a second isolation trench 58 adjoining a memory cell active region of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench.

Claim 1 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 2, Mehta's first isolation trench 62 is formed to a depth of from about 2500 to about 5000 angstroms (see column 5, lines 17-20).

Claim 2 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 3, Mehta's second isolation trench 58 is formed to a depth of from about 4000 to about 9000 angstroms (see column 5, lines 20-22).

Claim 3 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 4, Mehta's product further comprises a first isolation region 78 formed within the first isolation trench 62 and a second isolation region 78 formed within the second isolation trench 58.

Claim 4 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to independent claim 7, Mehta discloses a method for fabricating an embedded semiconductor product (see the entire patent, including the Figs. 5-9 disclosure together with the Technical Field, Background and Summary) comprising: providing a semiconductor substrate 40; forming a first isolation trench 62 adjoining a logic cell active region of the semiconductor substrate (note column 5, lines 4-7); and forming a second isolation trench 58 adjoining a memory cell active region of the semiconductor substrate, wherein the second isolation trench is deeper than the first isolation trench.

Claim 7 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 8 (which is presumed to depend on independent method claim 7, as per the above rejection of claim 8 under 35 U.S.C. 112, second

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paragraph), Mehta's semiconductor substrate 40 is a silicon semiconductor substrate (see column 4, lines 31-32).

Claim 8 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 9 (which is presumed to depend on independent method claim 7, as per the above rejection of claim 9 under 35 U.S.C. 112, second paragraph), Yan's first isolation trench 62 is formed to a depth of from about 2500 to about 5000 angstroms (see column 5, lines 17-20).

Claim 9 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 10 (which is presumed to depend on independent method claim 7, as per the above rejection of claim 10 under 35 U.S.C. 112, second paragraph), Mehta's second isolation trench 64 is formed to a depth of from about 5000 to about 6000 angstroms (see column 5, lines 20-22).

Claim 10 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 11 (which is presumed to depend on independent method claim 7, as per the above rejection of claim 11 under 35 U.S.C. 112, second paragraph), Mehta's product further comprises a first isolation region 78 formed within the first isolation trench 62 and a second isolation region 78 formed within the second isolation trench 58.

Claim 11 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to independent claim 14, Mehta discloses a method for fabricating an embedded semiconductor product (see the entire patent, including the Figs. 5-9 disclosure together with the Technical Field, Background and Summary) comprising:

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providing a semiconductor substrate 40; forming simultaneously a first isolation trench 62 adjoining a logic cell active region of the semiconductor substrate (note column 5, lines 4-7) and a second isolation trench 62/58 adjoining a memory cell active region of the semiconductor substrate; and further etching the second isolation trench but not the first isolation trench such that the second isolation trench is deeper than the first isolation trench.

Claim 14 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 15 (which is presumed to depend on independent method claim 14, as per the above rejection of claim 15 under 35 U.S.C. 112, second paragraph), Mehta's semiconductor substrate 40 is a silicon semiconductor substrate (see column 4, lines 31-32).

Claim 15 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 16 (which is presumed to depend on independent method claim 14, as per the above rejection of claim 16 under 35 U.S.C. 112, second paragraph), Yan's first isolation trench 62 is formed to a depth of from about 2500 to about 5000 angstroms (see column 5, lines 17-20).

Claim 16 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

With respect to dependent claim 17 (which is presumed to depend on independent method claim 14, as per the above rejection of claim 17 under 35 U.S.C. 112, second paragraph), Mehta's second isolation trench 58 is formed to a depth of from about 4000 to about 9000 angstroms (see column 5, lines 20-22).

Claim 17 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

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With respect to dependent claim 18 (which is presumed to depend on independent method claim 14, as per the above rejection of claim 18 under 35 U.S.C. 112, second paragraph), Mehta's product further comprises a first isolation region 78 formed within the first isolation trench 62 and a second isolation region 78 formed within the second isolation trench 58.

Claim 18 is thus rejected under 35 U.S.C. 102(e) as being anticipated by Mehta.

Claims 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not disclose or suggest the allowable semiconductor device taken as a whole, including the storage capacitor plate layer.

Registered practitioners can telephone the examiner at (571) 272-1843. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the Application/Control (Serial) Number. Technology Center 2800's general telephone number is (571) 272-2800.

  
Mark V. Prenty  
Primary Examiner